AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims

1.-8. (cancelled).

9. (new) A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming an isolation groove in a silicon surface of a first major surface of a wafer, so as to divide the silicon surface into two regions which are to be first and second regions;

(b) forming a first insulating film of silicon oxide by chemical vapor deposition, the first insulating film covering the silicon surface;

(c) planarizing the silicon surface covered with the first insulating film by removing the first insulating film outside the isolation groove with chemical mechanical polishing;

(d) forming two gate electrodes, to be N- and P-type gate electrodes, respectively over the first and second regions, each of said two gate electrodes having a silicon film to be a polysilicon conductive film;

(e) forming N-type source and drain regions in the first region, said N-type source and drain regions to constitute a first insulated gate field effect transistor together with the N-type gate electrode and a pair of first insulating side walls;

(f) forming P-type source and drain regions in the second region, said P-type source and drain regions to constitute a second insulated gate field effect transistor together with the P-type gate electrode and a pair of second insulating side walls;

(g) exposing surface portions of the silicon surface over said N-type and P-type source regions and drain regions;

(h) depositing a Co film covering at least the exposed surface portions, by sputtering, from a Co sputtering target which, apart from carbon and oxygen impurities, is at least 99.99 wt.% pure, wherein a sum of Fe and Ni in the Co sputtering target is not greater than 50 ppm by weight, and wherein the sputtering is performed in such a manner that the composition of the deposited Co film is substantially the same as that of the Co sputtering target;

(i) performing first rapid thermal annealing at a first temperature to the first major surface formed with the Co film so as to form Co monosilicide films over the surface portions, leaving a remaining Co film not formed into Co monosilicide, wherein the first temperature is a temperature that creep-up across the first and second insulating side walls substantially does not take place;

(j) removing the remaining Co film, remaining over the first major surface, by wet etching; and

(k) after step (j), performing second rapid thermal annealing at a second temperature higher than the first temperature to the first major surface so as to form Co disilicide films over the surface portions.

10. (new) A method of fabricating a semiconductor integrated circuit device according to claim 9, wherein the first temperature is not higher than 525°C.

11. (new) A method of fabricating a semiconductor integrated circuit device according to claim 10, wherein the Co sputtering target includes a sum of Fe and Ni which is not greater than 10 ppm by weight.

12. (new) A method of fabricating a semiconductor integrated circuit device according to claim 10, wherein said Co sputtering target, apart from carbon and oxygen impurities, is 99.999 wt. % pure.

13. (new) A method of fabricating a semiconductor integrated circuit device according to claim 10, wherein the first temperature is not lower than 475°C.

14. (new) A method of fabricating a semiconductor integrated circuit device according to claim 10, wherein the semiconductor integrated circuit device is designed under design rules not larger than 0.25 μm.

15. (new) A method of fabricating a semiconductor integrated circuit device according to claim 11, wherein the Co sputtering target, apart from carbon and oxygen impurities, is 99.999 wt.% pure.

16. (new) A method of fabricating a semiconductor integrated circuit device according to claim 15, wherein the second temperature is from 650° to 800°C.

17. (new) A method of fabricating a semiconductor integrated circuit device according to claim 9, wherein said P-type gate electrode is doped with boron.